

Features

- Phase Controlled Thyristor Ignition
- Triggering with Time Delay
- Repetition Time Delay
- Supply Current ≤ 2 mA
- Mains Supply via Resistor

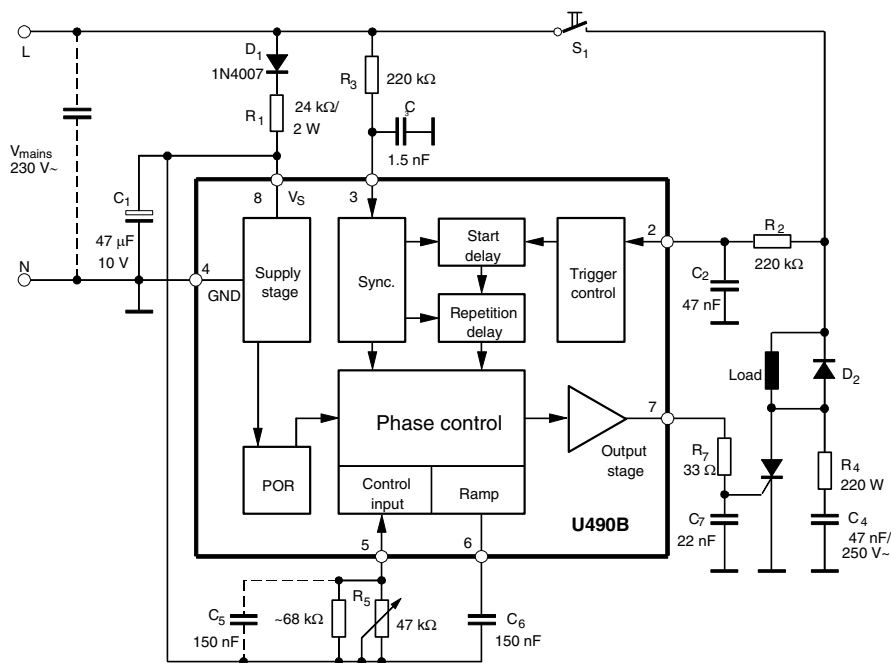
Applications

- Electric Stapler Devices

Description

The monolithic integrated bipolar circuit, U490B, is a one-shot power control circuit, designed to control the thyristor which is mainly used in electric stapler devices. The IC is preferred to realize a one-shot phase control, where any phase angle, thus any intensity of the load voltage is adjustable. After successful triggering and the following delay time, an ignition pulse at the output is released. Further triggering is only possible after the delay time elapses.

Figure 1. Block Diagram

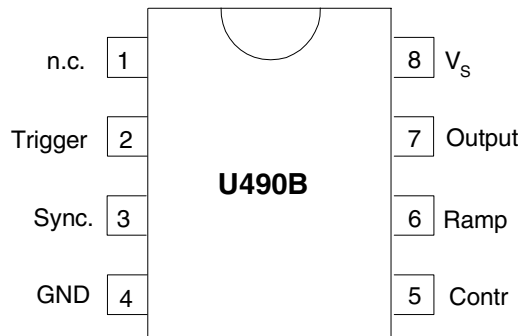


One-shot Phase Control IC

U490B

Pin Configuration

Figure 2. Pinning DIP8/SO8



Pin Description

Pin	Symbol	Function
1	n.c.	Not connected
2	Trigger	Triggering
3	Sync.	Synchronization
4	GND	Ground
5	Contr	Control input
6	Ramp	Ramp
7	Output	Output
8	V _S	Supply voltage

Supply, Pin 8

The internal voltage limiter enables a simple supply from the mains via series resistor R_1 . The supply voltage between pin 8 (V_S) and ground (pin 4) builds up via R_1 and is smoothed by the capacitor C_1 .

The series resistor R_1 can be calculated as follows:

$$R_{1\max} \approx 0.85 \times \frac{V_{\text{mains}} - V_{S\max}}{2 \times I_{\text{tot}}} \quad \text{where}$$

V_{mains} Mains supply voltage

$V_{S\max}$ Maximum supply voltage

I_{tot} $I_{S\max} + I_X$

$I_{S\max}$ Maximum current consumption of the IC

I_X Current consumption of the external components

Phase Control, Pins 3, 5 and 6

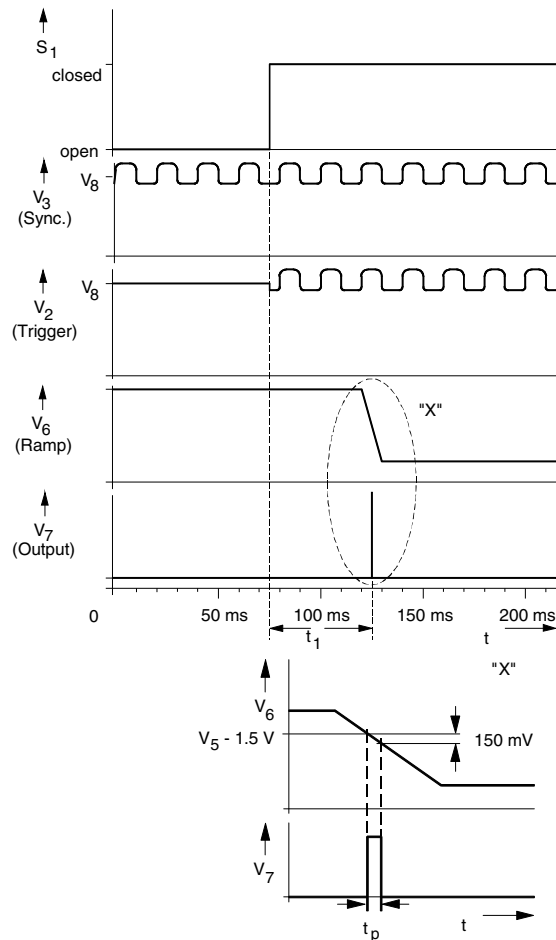
The circuit is synchronized with mains supply through pin 3. As long as the switch S_1 is open, the circuit is in wait state, i.e., the capacitor C_6 (150 nF) is discharged and is kept in this state (High level). When the switch S_1 is closed, there is a current flow in pin 2 which is evaluated by the circuit. If this current flows after the delay time elapses, the phase control is released. The capacitor C_6 is then charged with $I_6 + 100 \mu\text{A}$ towards ground. At the same time, a current of $\approx 100 \mu\text{A}$ flows into pin 5, which results in a voltage drop across resistor R_5 . The control voltage V_5 is then 1.5 V lower internally.

The output stage is released when the ramp voltage V_6 is equal to $(V_5 - 1.5 \text{ V})$. When the voltage difference is $\approx 150 \text{ mV}$, it is again turned-off.

The result is an output pulse, whose phase shift to the zero crossing of the mains voltage is determined by the resistor R_5 at the control input pin 5 (see Figure 3). The capacitor C_6 is charged to a value of $\approx 1.5 \text{ V}$. This value is kept until the switch S_1 opens again and the repetition delay time has elapsed.

The circuit is released when four periods of the line voltage have expired after build-up of the operating voltage, before the switch S_1 is closed.

Figure 3. Signal Characteristics



Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Reference point pin 4 (GND), unless otherwise specified

Parameters	Symbol	Value	Unit
Supply current, pin 8	I_S	30	mA
$t \leq 10 \mu s$	i_s	150	mA
Output stage			
Input voltage, pin 7	V_I	-0.5 to V_S	V
Input current, pins 2 and 3	$\pm I_I$	5	mA
$t \leq 1 ms$	$\pm I_I$	30	mA
Input voltage, pins 5 and 6	V_I	0 to V_g	V
Junction temperature	T_j	+125	°C
Ambient temperature	T_{amb}	-10 to +100	°C
Storage temperature range	T_{stg}	-40 to +125	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	110	K/W
DIP8	R_{thJA}	220	K/W
SO8 on p.c.	R_{thJA}	140	K/W
SO8 on ceramic	R_{thJA}		

Electrical Characteristics

$V_S = 7 V$, $T_{amb} = 25^\circ C$, reference point pin 4 (GND), unless otherwise specified

Parameters	Test Conditions/ Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage limitation	$I_S = 3 mA$ Pin 8	V_S	7.2	8.2	9.2	V
	$I_S = 30 mA$	V_S	7.4	8.4	9.4	V
Current consumption	$V_S = 7 V$ Pin 8	I_S			2	mA
Voltage Monitoring						
Switch-on threshold	Pin 8	V_{Son}		5		V
Switch-off threshold		V_{Soff}		3		V
Synchronization						
Voltage limitation	$I_3 = +1 mA$ Pin 3 – 8	V_{lim}		1.5		V
	$I_3 = -1 mA$	$-V_{lim}$		0.75		V
Switch-on threshold	Pin 3	I_{Ton}		120		μA
Switch-off threshold		I_{Toff}		35		μA
Trigger Input						
Voltage limitation	$I_2 = +1 mA$ Pin 2 – 8	V_{lim}		1.5		V
	$I_2 = -1 mA$	$-V_{lim}$		0.75		V
Switch-on threshold	Pin 2	I_{Ton}		120		μA
Switch-off threshold		I_{Toff}		35		μA
Start delay time	$f_{mains} = 50 Hz$ Pin 2–7	t_1	40		60	ms
Repetition delay time		t_2	60		80	ms

Electrical Characteristics (Continued)

$V_S = 7\text{ V}$, $T_{\text{amb}} = 25^\circ\text{C}$, reference point pin 4 (GND), unless otherwise specified

Parameters	Test Conditions/ Pins	Symbol	Min.	Typ.	Max.	Unit
Phase Control						
Control input:	Pin 5					
Input voltage range		V_I	2		V_S	V
Input current	$2\text{ V} \leq V_5 \leq V_8$	I_I	50	90	130	μA
Ramp						
Charge current	$2\text{ V} \leq V_6 \leq V_8 - 0.5\text{ V}$	I_{ch}	50	90	130	μA
Discharge current	$V_5 = 4\text{ V}$	$-I_{\text{dis}}$	2			mA
Phase Shift		t_{dmax}		7		ms
	$C_6 = 150\text{ nF}$, $V_5 = 2\text{ V}$ $V_5 = V_8$, Pin 7–5	t_{dmin}		600		μs
Output Stage, $V_7 + 0\text{ V}$, Pin 7						
Output reverse current	Status OFF	$\pm I_{\text{O(r)}}$			10	μA
Output current	Status ON	$-I_{\text{O}}$	100			mA
Pulse width	$C_6 = 150\text{ nF}$ (see Figure 3 on page 3)	t_p	100	200	300	μs

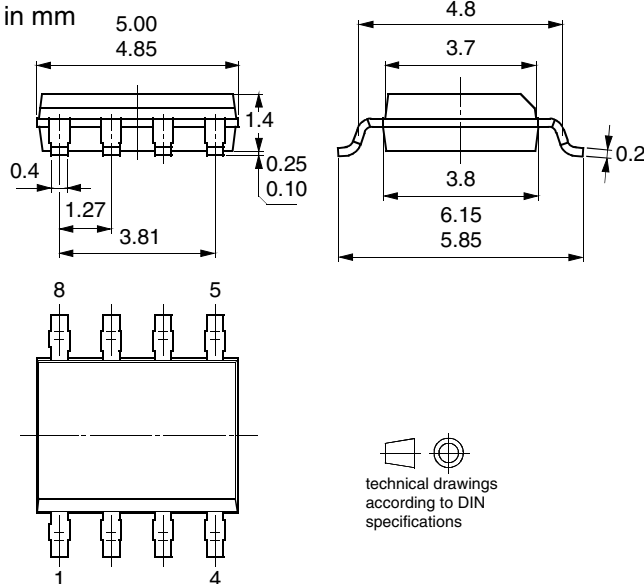
Ordering Information

Extended Type Number	Package	Remarks
U490B-x	DIP8	Tube
U490B-xFP	SO8	Tube
U490B-xFPG3	SO8	Taped and reeled

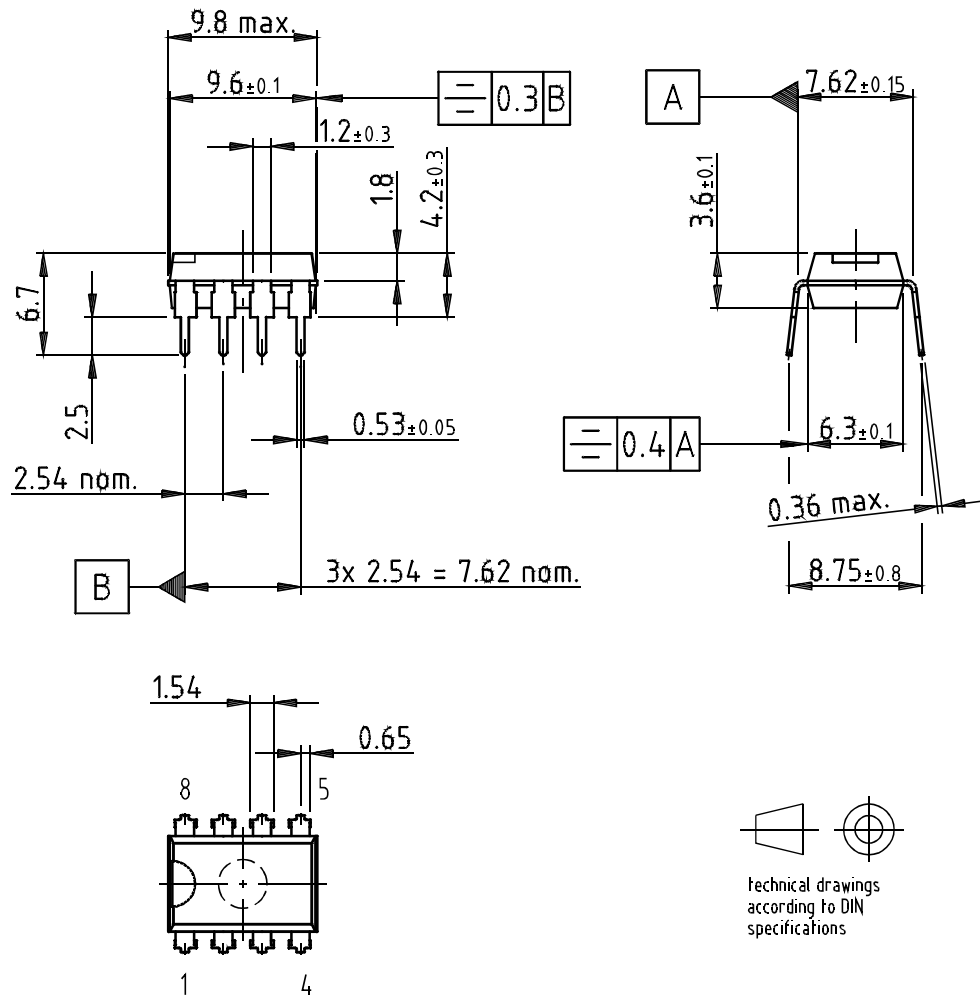
Package Information

Package SO8

Dimensions in mm



Package: DIP 8
Dimensions in mm



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